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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,535	09/22/2003	Paul F. Illegems	5707-0410	9954
7590	06/30/2005			
Jeffrey C. Hood Meyertons, Hood, Kivlin, Kowert & Goetzel PC P.O. Box 398 Austin, TX 78767				
EXAMINER				
ENGLUND, TERRY LEE				
ART UNIT		PAPER NUMBER		
2816				

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/667,535

Applicant(s)

ILLEGEMS, PAUL F.

Examiner

Terry L. Englund

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 April 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16, 18, 19, 25 and 26 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1, 5, 8, 9, 13, 15, 16, 18, 19, 25, and 26 is/are rejected.
7) ☒ Claim(s) 2-4, 6, 7, 10-12 and 14 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 07 April 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

Response to Amendment/Drawing

The amendment and drawing submitted on Apr 7, 2005 were reviewed and considered with the following results:

The replacement sheet for Fig. 7 has been approved by the examiner. It overcomes its typo related objection, which has now been withdrawn.

The amended paragraph overcame its objection that was described in the previous Office Action. Therefore, that objection has also been withdrawn.

Cancelled claims 17, and 20-24 rendered their corresponding objection(s) and/or rejection(s) moot.

The amended claims overcame most of the claim objections described in the previous Office Action. However, some of the objections were either not addressed/corrected, or satisfactorily addressed/corrected (e.g. with respect to "variations" or "emitters"). Also, some amended changes created new objections. Therefore, all active objections are described later under the appropriate section, wherein the other objections from the previous Office Action that have been satisfactorily overcome have been withdrawn.

The amended claims, and/or the applicant's arguments, overcame the rejections of claims 1, 5, 8-9, 13, 15-16, and 18-19 under 35 U.S.C. 102(b) with respect to Wu. Since the reference of Wu does not clearly show or disclose the second component of the voltage as recited within the independent claims, those prior art rejections have now been withdrawn.

However, several other prior art references (found during a recent update search) have been interpreted as meeting the recited limitations of at least some of the claims, with respect to

Art Unit: 2816

the broadest reasonable interpretations of the claimed limitations. Therefore, these rejections are described later under the appropriate claim rejection sections.

Claim Objections

Claims 5, 7-16, 18-19, and 25-26 are objected to because of the following informalities:

Since each of independent claims 1, 9, and 16 recite at least one limitation with respect to variations in operating temperature, and/or transistor fabrication parameters, it is suggested the term --the-- be added prior to “variations” in claims 5 (i.e. lines 3 and 4), 8 (lines 2 and 3), 9 (line 11), 13 (lines 3 and 4), 15 (line 3), 16 (line 12), 18 (line 3), and 26 (lines 2 and 3). These changes will clearly relate the second recited version of “variations” back to their corresponding initial recitation of “variations” phrase(s). Claim 7, line 2 “emitters” should be --sources-- because NMOS transistors do not have emitters. Claim 16, line 12 should have --the-- added prior to “operating” since line 5 of the same claim has already recited “operating temperature.”

Dependent claims carry over any objection(s) from any claim(s) upon which they depend.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Art Unit: 2816

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 5, 9, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kraus, a reference found during a recent update search. Fig. 6 shows a device comprising voltage level detector 24 comprising NMOS tail current transistor m22; and voltage generator 20, coupled to the gate of tail current transistor m22, for applying voltage vref to that gate. One of ordinary skill in the art would understand voltage vref comprises a first component (e.g. corresponding to the threshold of diode-connected NMOS transistor q6) approximately equal to a threshold voltage of the NMOS transistors in the device, and a second component (e.g. the voltage dropped across resistor r4 and transistor q6) that is approximately constant with respect to variations in operating temperature and/or variations in transistor fabrication parameters (e.g. see column 4, lines 24-28). Therefore, claim 1 is anticipated. Since transistor q6 is diode-connected, and its voltage drop corresponds to the diode's threshold voltage, it would provide the minimum voltage required to turn on tail current transistor m22, and claim 5 is anticipated. [Note: It is understood the threshold of a diode is substantially constant with respect to temperature and fabrication variations.] Interpreting Fig. 6 in a slightly different manner, voltage level detector 24 comprises differential amplifier M17-M22, which comprises NMOS tail current transistor m22. Therefore,

Art Unit: 2816

claims 9 and 13 are anticipated for the same type reasoning as applied to claims 1 and 5, respectively described above.

[Note: Although tail current transistor m22 of Kraus shows a small circle at its gate, which could identify the transistor as a PMOS transistor, that circle is considered an oversight within the figure. Transistor m22 is also identified with “n”, and an arrow pointing in at the transistor’s backgate section. These identifiers correspond to the other NMOS transistors shown within the figure, and well known by one of ordinary skill in the art was identifying the corresponding MOS transistor as an N-type.]

Claims 1, 5, 9, and 13 are also rejected under 35 U.S.C. 102(e) as being anticipated by Nakai, another reference found during the recent update search. Nakai’s Fig. 2 shows a device comprising voltage level detector 40 comprising NMOS tail current transistor N3; and voltage generator 32, coupled to the gate of tail current transistor N3, for applying voltage VBIAS to that gate. One of ordinary skill in the art would understand voltage VBIAS comprises a first component (e.g. corresponding to the threshold of diode-connected NMOS transistor N8) approximately equal to a threshold voltage of the NMOS transistors in the device, and a second component (e.g. voltage V_{bem} , at node W5, corresponds to the voltage dropped across the parallel coupled bipolar transistors $Q_{n+2} - Q_{n+m+1}$ that is approximately constant with respect to variations in operating temperature and/or variations in transistor fabrication parameters (e.g. see related column 10, lines 48-57)). Therefore, claim 1 is anticipated. Since transistor N8 is diode-connected, and its voltage drop corresponds to the diode’s threshold voltage, it would provide the minimum voltage required to turn on tail current transistor N3, and claim 5 is anticipated. [Note: It is understood the threshold of a diode is substantially constant with respect

Art Unit: 2816

to temperature and fabrication variations.] Interpreting Fig. 6 in a slightly different manner, voltage level detector 40 comprises differential amplifier 40, which comprises NMOS tail current transistor N3. Therefore, claims 9 and 13 are anticipated for the same type reasoning as applied to claims 1 and 5, respectively described above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus as applied to their corresponding independent claim 1 and 9 above, and claims 16, 18-19, and 25-26, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus. The device of Kraus shows/discloses a device with a voltage level detector/differential amplifier having an NMOS tail current transistor; and a voltage generator for delivering a voltage (with first/second components) to the gate of the tail current transistor. However, the reference does not clearly show or disclose the trip point of the voltage level detector is substantially constant as recited within claims 8 and 16; the offset voltage of the differential amplifier is substantially constant as recited within claims 15 and 26; and the tail current is proportional to a beta in the NMOS process. With a substantially constant voltage v_{ref} applied to the gate of tail current transistor m22, which has operating characteristics corresponding to transistor q6 (as well as the other NMOS transistors within the device), it would be obvious to one of ordinary skill in the art that the trip point of voltage level detector 24 would be considered substantially constant over variations of

Art Unit: 2816

temperature and transistor fabrication parameters, rendering claim 8 obvious. For similar reasons, the offset voltage of differential amplifier m17-m22 would be considered substantially constant, and claim 15 is rendered obvious. Interpreting Fig. 6 in a different manner, the current flowing through resistor r4 effectively generates a constant reference voltage; diode-connected transistor q6 generates a threshold voltage of an NMOS process over variations in operating temperature/transistor fabrication parameters; M14,r4,q6 generate a composite voltage that is the sum of the constant voltage (across r4) and the threshold voltage component (across q6), and this composite voltage is applied to the gate of tail current transistor m22 of voltage level detector 24. Since a substantially constant composite voltage v_{ref} is applied to the gate of tail current transistor m22, which has operating characteristics corresponding to transistor q6 (as well as the other NMOS transistors within the device), it would be obvious to one of ordinary skill in the art that the trip point of voltage level detector 24 would be considered substantially independent over variations of temperature and transistor fabrication parameters, and therefore be substantially constant. This renders claim 16 obvious. As the threshold voltage component (of q6) would correspond to the threshold of tail current transistor m22, once the overall device has reached a minimum temperature and operating power supply level, which allows q6 to begin conducting current, the threshold voltage component will turn on the tail current transistor despite the variations in temperature and transistor fabrication parameters, rendering claim 18 obvious. Since tail current transistor m22 is an NMOS transistor, its tail current, which is related to the constant reference voltage component applied to the gate of the tail current transistor, will inherently be proportional to a beta for the NMOS process (e.g. used to fabricate NMOS transistor m22 and the other NMOS transistors within the device). This renders claim 19

Art Unit: 2816

obvious. Voltage level detector 24 is one type of differential amplifier (e.g. see m17-m22), and claim 25 is rendered obvious. As previously described above, the offset voltage of the differential amplifier will be considered as substantially constant despite variations in temperature and transistor fabrication parameters. Therefore, claim 26 is also rendered obvious.

Claims 8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai as applied to their corresponding independent claim 1 and 9 above, and claims 16, 18-19, and 25-26, are also rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai. Nakai shows/discloses a device with a voltage level detector/differential amplifier having an NMOS tail current transistor; and a voltage generator for delivering a voltage (with first/second components) to the gate of the tail current transistor. However, the reference does not clearly show or disclose the trip point of the voltage level detector is substantially constant as recited within claims 8 and 16; the offset voltage of the differential amplifier is substantially constant as recited within claims 15 and 26; and the tail current is proportional to the NMOS process. With a substantially constant voltage VBIAS applied to the gate of tail current transistor N3, which has operating characteristics corresponding to transistor N8 (as well as the other NMOS transistors within the device), it would be obvious to one of ordinary skill in the art that the trip point of voltage level detector would be considered substantially constant over variations of temperature and transistor fabrication parameters, rendering claim 8 obvious. For similar reasons, the offset voltage of differential amplifier 40 would be considered substantially constant, and claim 15 is rendered obvious. Interpreting Fig. 2 in a different manner, parallel connected bipolar transistors $Q_{n+2} - Q_{n+m+1}$ generate constant reference voltage V_{bem} ; diode-connected transistor N8 generates a threshold voltage of an NMOS process over variations in operating temperature/transistor

Art Unit: 2816

fabrication parameters; and 32 generates composite voltage VBIAS that is the sum of the constant voltage (across the parallel bipolar transistors) and the threshold voltage component (across N8), and composite voltage VBIAS is applied to the gate of tail current transistor N3 of voltage level detector 40. Since a substantially constant composite voltage VBIAS is applied to the gate of tail current transistor N3, which has operating characteristics corresponding to transistor N8 (as well as the other NMOS transistors within the device), it would be obvious to one of ordinary skill in the art that the trip point of voltage level detector 40 would be considered substantially independent over variations of temperature and transistor fabrication parameters, and therefore be substantially constant. This renders claim 16 obvious. As the threshold voltage component (of N8) would correspond to the threshold of tail current transistor N3, once a minimum temperature and power supply level has been reached that will allow N8 to begin conducting current, the threshold voltage component will turn on the tail current transistor despite the variations in temperature and transistor fabrication parameters, rendering claim 18 obvious. Since tail current transistor N3 is an NMOS transistor, its tail current, which is related to the constant reference voltage component applied to the gate of the tail current transistor, will inherently be proportional to a beta for the NMOS process (e.g. used to fabricate NMOS transistor N3 and the other NMOS transistors within the device). This renders claim 19 obvious. Voltage level detector 40 is one type of differential amplifier, and claim 25 is rendered obvious. As previously described above, the offset voltage of the differential amplifier will be considered as substantially constant despite variations in temperature and transistor fabrication parameters. Therefore, claim 26 is also rendered obvious.

No claim is allowable as presently written.

Art Unit: 2816

Claims 17 and 20-24 have been cancelled.

Allowable Subject Matter

However, claims 2-4, 6-7, 10-12, and 14 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the device comprises: 1) the first component of the voltage being produced by a diode-connected NMOS transistor and a constant current source as recited within claims 2 (upon which claims 3-4 depend) and 10 (upon which claims 11-12 depend); 2) the second component is a constant effective voltage, wherein the tail current is proportional to beta according to the equation recited within claims 6 and 14; and 3) the channel width to length ratios of the first/second transistors within the differential amplifier are different as recited within claim 7.

Response to Arguments

The applicant's arguments within the amendment filed Apr 7, 2005, with respect to the rejection(s) of claim(s) 1, 5, 8-9, 13, and 15-16, under 35 U.S.C. 102(b), have been fully considered and are persuasive. Therefore, the prior art rejections described in the previous Office Action have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the references of Nakai and Kraus, both references found during a recent update search.

THIS ACTION IS MADE FINAL. The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2816

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743.

The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.


The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
24 June 2005


TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

IN THE DRAWINGS:

The attached replacement sheet contains a formal drawing that includes changes to FIG. 7. This sheet replaces the originally filed sheet containing the same figure.

Attachment: 1 replacement sheet and 1 sheet illustrating the change to FIG. 7 of the original drawing.

Approved
6.23.05
TLE



Approved
6.23.05
TLE

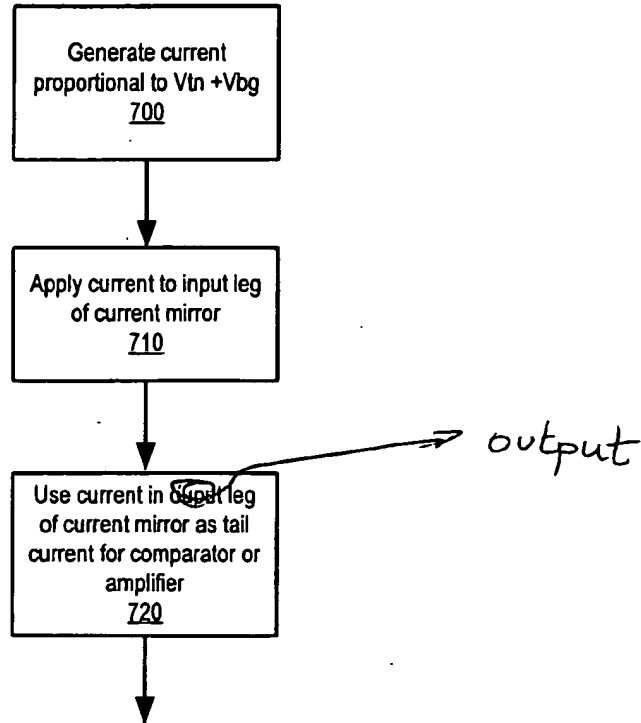


FIG. 7

Approved
6.23.05
TLE

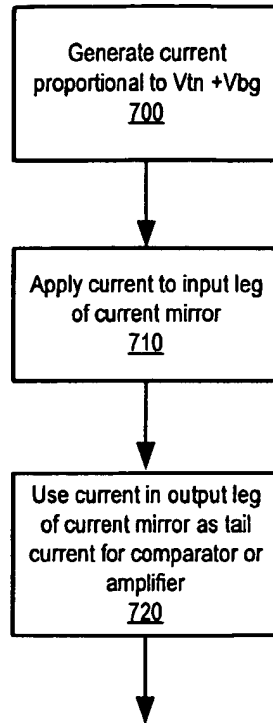


FIG. 7

(Replacement Sheet)